Notice of Allowability	Application No.	Applicant(s)
	10/759,188	MITARASHI, MUTSUMI
	Examiner	Art Unit
	Angela M. Lie	2821

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/20/2004*.

2. ☒ The allowed claim(s) is/are *1-14*.

3. ☒ The drawings filed on *20 January 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 01/20/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *04/28/2005* .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TUYET VO
PRIMARY EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ken Fields on April 28, 2005.

The application has been amended as follows:

On page 53:

In claim 1, line 15, deleted "impressed", before "gate", added --a--, before "with said first", added --supplied--, deleted --control--.

In claim 1, line 17, deleted "impressed", before "gate of said first", added --a--.

In claim 1, line 18, before "with said first", added --supplied--, deleted "control".

In claim 1, line 23, deleted "impressed", before "gate of said second", added --a--, before "with said second", added --supplied--.

In claim 1, line 25, deleted "impressed", before "gate of said second", added --a--.

In claim 1, line 26, before "with said second", added --supplied--.

On page 54:

In claim 1, line 3, before "overvoltage protecting circuit", --a-- changed to --an--, deleted "third p-channel type MOS".

In claim 1,line 4, deleted "transistor connected", before "drain of said third", added --a--, before "with third", added --connected--.

In claim 1, line 5, deleted "impressed", before "source of said third", added --a--, before "with", added --supplied--.

In claim 1, line 6, deleted "third n-channel type MOS transistor connected".

In claim 1, line 7, before "drain of said third", added --a--, before "with third output node", added --connected--.

In claim 1, line 8, deleted "impressed", before "source of said third", added --a--, before "with said third", added --supplied--.

In claim 1, line 9, deleted "said overvoltage protecting circuit impressed".

In claim 1, line 11, before "with said low voltage", added --is supplied--, before "puts out a fourth signal", added --and--.

On page 56:

In claim 8, line 12, deleted "impressed", before "with said first", added --supplied--, deleted "control".

In claim 8, line 14, deleted "impressed".

In claim 8, line 15, before "with said second", added --supplied--, deleted "control".

In claim 8, line 20, deleted "impressed", before "with said third", added --supplied--.

In claim 8,line 22, deleted "impressed".

In claim 8, line 23, before "with said fourth control", added --supplied--.

On page 57:

In claim 8,line 1, before "overvoltage protecting circuit", --a-- changed to --an--.

In claim 8, line 2, deleted "impressed", before "with said", added --supplied--.

In claim 8, line 3, deleted "connected", before "drain of said third", added --a--, before "with", added --connected--.

In claim 8, line 4, deleted "impressed".

In claim 8, line 5, before "with said fourth signal", added --supplied--.

In claim 8, line 6, deleted "connected", before "drain of said", added --a--, before "with third output", added --connected--.

In claim 8, line 7, deleted "said overvoltage protecting circuit impressed".

In claim 8, line 9, before "with said low voltage", added --is supplied--, before "puts put a fifth signal", added --and--.

The Examiner's amendment has been made in order to comply with the 35 U.S.C 112, second paragraph and to place the application in a condition for allowance.

2. Claims 1-14 are allowed.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

As to claim 1, the cited art of record fails to teach a semiconductor integrated comprising a level transforming circuit inputted with the first control signal, inputted with the inverse signal, putting out a first signal having amplitude between the low voltage and a high voltage higher than the low voltage, a first buffer circuit which has a first p-channel type MOS transistor connected between the high voltage of electricity source and first output node, a gate of the first p-channel type MOS transistor supplied with first

signal, and which has first n-channel type MOS transistor connected between the first output node and the ground, a gate of the first n-channel type MOS transistor supplied with the first signal, and wherein the first buffer circuit puts out a second signal having amplitude between the high voltage and the low voltage to the first output node; a second buffer circuit which has a second p-channel type MOS transistor connected between the low voltage of electricity source and second output node, a gate of the second p-channel type MOS transistor supplied with the second control signal, and which has second n-channel type MOS transistor connected between the second output node and the ground, a gate of the second n-channel type MOS transistor supplied with the second control signal, and wherein the second buffer circuit puts out a third signal having amplitude between the low voltage and the ground to the second output node; and an overvoltage protecting circuit which has a drain of the third p-channel type MOS transistor connected with third output node, a source of the third p-channel type MOS transitor supplied with the second signal, and which has a drain of the third n-channel type MOS transistor connected with third output node, a source of the third n-channel type MOS transistor connected with third output node, a source of the third n-channel type MOS transistor supplied with the third signal, and wherein each gate of the third p-channel type MOS transistor and the third n-channel type MOS transistor is supplied with the low voltage in common, and puts out a fourth signal having amplitude between the high voltage and the ground to the third output node. All those limitations are clearly disclosed in the body of claim 1.

As to claims 2-7, those claims are allowable by the virtue of their dependency on claim 1.

As to claim 8, the cited art of record fails to teach a semiconductor integrated circuit comprising: a first level transforming circuit inputted with the first control signal, inputted with the first inverse signal, putting out first signal having amplitude between the low voltage and a high voltage, a second level transforming circuit inputted with the second control signal, inputted with the second inverse signal, putting out a second signal having amplitude between the low voltage and a high voltage, a first buffer circuit which has first p-channel type MOS transistor, gate of the first p-channel type MOS transistor supplied with the first signal, connected the high voltage of electricity source and first output node, and which has first n-channel type MOS transistor gate of the first n-channel type MOS transistor supplied with the second signal, connected between the first output node and the ground, and wherein the first buffer circuit puts out a third signal having amplitude between the high voltage and the low voltage to the first output node; a second buffer circuit which has second p-channel type MOS transistor supplied with the third control signal, connected between the low voltage of electricity source and second output node, and which has second n-channel type MOS transistor gate of the second n-channel type MOS transistor supplied with the fourth control signal, connected between the second output node and the ground, and wherein the second buffer circuit puts out fourth signal having amplitude between the low voltage and the ground to the second output node; and an overvoltage protecting circuit which has third p-channel type MOS transistor source of the third p-channel type MOS transistor supplied with the

third signal, a drain of the third p-channel type MOS transistor connected with third output node, and which has a third n-channel type MOS transistor source of the third n-channel type MOS transistor supplied with the fourth signal, a drain of the third n-channel type MOS transistor connected with third output node, and wherein each gate of the third p-channel type MOS transistor and the third n-channel type MOS transistor is supplied with the low voltage in common, and puts out fifth signal having amplitude between the high voltage and the ground to the third output node. All those limitations are clearly stated in the body of claim 8.

As to claims 9-14, those claims are allowable by the virtue of their dependency on claim 8.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

The Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 5880617 discloses a level conversion circuit
- US 6323704 discloses a multiple voltage compatible I/O buffer
- US 6366141 discloses a semiconductor driver circuit utilizing substrate voltage control

- US 6392439 discloses a level conversion circuit and semiconductor integrated circuit device employing the level conversion circuit
- Us 6483766 discloses an interface circuit for using in high-speed semiconductor device and interfacing method
- US 6504400 discloses a level conversion circuit and semiconductor integrated circuit device employing the level conversion circuit.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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TUYET VO
PRIMARY EXAMINER